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Solution-Processable $LaZrO_x/SiO_2$ Gate Dielectric at Low Temperature of 180 °C for High-Performance Metal Oxide Field-Effect Transistors

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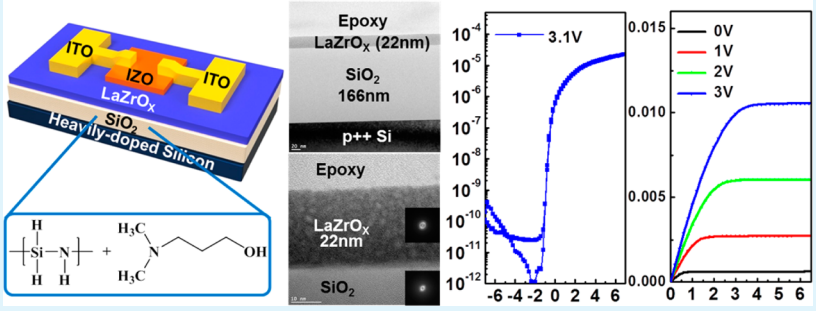
Supporting Information



ABSTRACT: Although solution-processable high-k inorganic dielectrics have been implemented as a gate insulator for high-performance, low-cost transition metal oxide field-effect transistors (FETs), the high-temperature annealing (>300 °C) required to achieve acceptable insulating properties still limits the facile realization of flexible electronics. This study reports that the addition of a 2-dimetylamino-1-propanol (DMAPO) catalyst to a perhydropolysilazane (PHPS) solution enables a significant reduction of the curing temperature for the resulting SiO_2 dielectrics to as low as 180 °C. The hydrolysis and condensation of the as-spun PHPS film under humidity conditions were enhanced greatly by the presence of DMAPO, even at extremely low curing temperatures, which allowed a smooth surface (roughness of 0.31 nm) and acceptable leakage characteristics (1.8×10^{-6} A/cm^2 at an electric field of 1MV/cm) of the resulting SiO_2 dielectric films. Although the resulting indium zinc oxide (IZO) FETs exhibited an apparent high mobility of 261.6 cm^2/(V s), they suffered from a low on/off current ($I_{ON/OFF}$) ratio and large hysteresis due to the hygroscopic property of silazane-derived SiO_2 film. The $I_{ON/OFF}$ value and hysteresis instability of IZO FETs was improved by capping the high-k $LaZrO_x$ dielectric on a solution-processed SiO_2 film via sol−gel processing at a low temperature of 180 °C while maintaining a high mobility of 24.8 cm^2/(V s). This superior performance of the IZO FETs with a spin-coated $LaZrO_x/SiO_2$ bilayer gate insulator can be attributed to the efficient intercalation of the 5s orbital of In^{3+} ion in the IZO channel, the good interface matching of IZO/$LaZrO_x$ and the carrier blocking ability of PHPS-derived SiO_2 dielectric film. Therefore, the solution-processable $LaZrO_x/SiO_2$ stack can be a promising candidate as a gate dielectric for low-temperature, high-performance, and low-cost flexible metal oxide FETs.

KEYWORDS: *solution process, silicon dioxide, lanthanum zirconium oxide, indium zinc oxide, field-effect transistor, low temperature*

1. INTRODUCTION

Transparent transition metal oxide (TMO) field-effect transistors (FETs) hold great promise for a range of electronic applications, including active-matrix liquid crystal displays (LCD), organic light-emitting diode displays (OLED), and flexible/transparent electronics owing to their high mobility, wide energy band gap (>3.0 eV), low temperature processing, good uniformity, and reasonable electrical stability. A variety of high-mobility TMO semiconductors, such as ZnO, InZnO, ZnSnO, InGaZnO, and InZnSnO, have been explored as channel materials using expensive vacuum-based deposition processes, such as sputtering, pulsed laser deposition, and atomic layer deposition.[1−5] In contrast, the solution processing of TMO semiconductors is a viable alternative because of the processing simplicity, low cost, and potentially high throughput. Therefore, low-temperature (<250 °C), solution-processable

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TMO TFTs have been developed by hydrolysis synthesis,[6] combustion process,[7] high pressure annealing,[8] and photochemical activation annealing.[9]

In contrast, solution-processable dielectric films have generally been overlooked in the search of high performance flexible TMO FETs, even though the semiconductor/insulator interface strongly affects charge transport, carrier trapping phenomena, and device instability. Thus far, the commercial production of InGaZnO FET-driven LCD and OLED display panels utilizes SiN_x or SiO_2 films as a gate insulator deposited by plasma-enhanced chemical vapor deposition (PECVD) at high temperatures (>350 °C). The development of new gate dielectric materials that offer both solution processing and low-temperature capability is an important and stringent objective for metal-oxide-based electronics, which enables the realization of low-cost flexible electronics, such as sensors, radio frequency identification tags, and backplane circuitry for active-matrix displays. For this reason, few studies have examined the solution processing of high-k dielectrics, such as Al_2O_3,[10,11] HfO_2,[12] Y_2O_3,[10,13] and ZrO_2,[14−16] for high-performance TFTs. The annealing temperature after the spin-coating of high-k metal oxide dielectrics has a profound effect on the electrical properties, which are affected significantly by unwanted impurities, such as carbon and hydroxyl group and uncompensated oxygen vacancies. High-temperature annealing (>300 °C), which is one of the main bottlenecks of flexible electronics on plastic substrates, is effective in removing the impurities and oxygen vacancies from high-k dielectric films leading to acceptable leakage and capacitance characteristics.[17] Therefore, it is important to identify a facile route for preparing high-quality dielectrics at low temperatures (<250 °C) without performance loss of the resulting FETs.

An alternative approach would be to implement the organic dielectric as a gate insulator, which has good insulating properties, excellent solution processability, and low-temperature processing.[18] On the other hand, the chemical dissimilarity of the interface between the organic dielectric and TMO semiconductor hinders carrier transport and can be an origin of carrier trap sites, which gives rise to inferior mobility and adverse field-effect properties.[19−22] Recently, a hybrid nanodielectric film comprised of inorganic/self-assembly monolayer stacks was proposed as a promising candidate gate insulator for high-performance, low-temperature TMO FETs.[23] Although this hybrid concept offers high capacitance, reasonable leakage current, good interface compatibility, and low operation voltage, the preparation of inorganic high-k metal oxides still requires an expensive vacuum-deposition step.[24]

This study reports high-performance TMO FETs with a solution-processed SiO_2 dielectric that is curable at temperatures as low as 180 °C. The spin-coated SiO_2 film was prepared using a new precursor of perhydropolysilazane (PHPS), which is a spin-on dielectric composed of silicon and nitrogen. The hydrolysis and subsequent condensation of PHPS in the presence of a catalyst of 2-dimetylamino-1-propanol (DMAPO) under humid conditions allowed the formation of high-quality SiO_2 films that exhibited good leakage characteristics, reasonable dielectric properties, and physical thickness controllability. To examine the interfacial compatibility between the solution-processable SiO_2 film and TMO semiconductor, FETs with an indium zinc oxide (IZO) channel layer were fabricated at the maximum process temperature of 180 °C. The bottom gate IZO FETs with the solution-processable SiO_2 dielectric can be produced to show an apparent high field-effect mobility of 261.6 $cm^2/(V\ s)$, subthreshold gate swing (SS) of 0.45 V/decade, threshold voltage (V_{TH}) of −3.3 V, and current ($I_{ON/OFF}$) ratio of 2×10^6. On the other hand, the SiO_2-only gated device suffered from a larger leakage current and batch-to-batch parameter variations due to the hygroscopic nature of the silazane-derived SiO_2 film. The leakage current characteristics and operation stress stability of the IZO FETs can be improved further by introducing a high-k $LaZrO_x$ dielectric, which can also be prepared by simple spin-coating and low temperature annealing at 180 °C. The IZO FETs with a stack of $LaZrO_x/SiO_2$ dielectric exhibited a low voltage driving of <5 V, a low SS factor of 0.16 V/decade, a high $I_{ON/OFF}$ ratio of 4×10^7, and a hysteresis-free good stability, whereas the high mobility of 24.8 $cm^2/(V\ s)$ was still maintained.

2. EXPERIMENTAL SECTION

2.1. Dielectric Film Preparation. The SiO_2 solution was prepared by dissolving perhydropolysilazane (PHPS, 1.90 M) and 2-dimetylamino-1-propanol ($C_5H_{13}NO$, 0.05 M) in 10 mL of di-*n*-butyl ether ($C_8H_{18}O$). The 2-dimetylamino-1-propanol (DMAPO) was used as a catalyst to initiate the hydrolysis and condensation reactions, thereby facilitating the formation of an amorphous SiO_2 network at low temperatures. The PHPS solution was spin-coated on bare Si substrates at 3000 rpm for 30 s. Before the PHPS coating, the bare Si was cleaned with acetone for 15 min followed by isopropyl alcohol for 15 min. The spin-coated PHPS films were baked on a hot plate for 5 min at 150 °C to remove the solvent. The PHPS films were then annealed under a moisture (H_2O) steam for 1 h at low temperatures of 180 and 250 °C. A precursor solution for the high-k $LaZrO_x$ dielectric was formulated by dissolving zirconium chloride ($ZrCl_4$, Aldrich) and lanthanum nitrate hexahydrate ($La(NO_3)_3{\cdot}6H_2O$, Aldrich) in ethanol, which was then stirred vigorously for 3 h at 50 °C until the solute had dissolved completely. The concentration of the precursor was 0.1 M, and the molar ratio of La/Zr was 1:2. The nitric acid and H_2O (1 M) were added as an oxidant into the $LaZrO_x$ precursor solution. The stirred LaZrO solution was filtered through a 0.2 μm syringe filter. The $LaZrO_x$ dielectric films were spin-coated on a bare Si or PHPS-derived SiO_2/Si substrate at 5000 rpm for 30 s, followed by drying at 100 °C on a hot plate for 10 min to eliminate the solvent. The $LaZrO_x$ films were annealed at 180, 250, 300, and 400 °C for 1 h under an electric furnace in an ambient atmosphere.

2.2. Material Characterization. The surface topography and roughness of the solution-processable dielectric films were analyzed by atomic force microscopy (AFM, JEOL, JSPM-5200) in tapping mode. The thickness of the SiO_2 and $LaZrO_x$ films was measured by scanning electron microscopy (SEM, Hitachi, S-4300) and transmission electron microscopy (TEM, JEOL, JEM-ARM200F). Fourier transform infrared (FTIR, Bruker, IFS66C/S, and HYPERION 3000) spectroscopy was used for the IR absorption spectra measurements of the PHPS-derived SiO_2 film, where bare silica glass was used as a reference. The chemical and structural properties of the PHPS-derived SiO_2 and $LaZrO_x$ dielectric films were examined by X-ray photoelectron spectroscopy (XPS, SIGMA PROBE, ThermoG, U.K.) and TEM, respectively.

2.3. Device Fabrication and Characterization. To examine the electrical properties, metal−insulator−metal capacitors were fabricated using sputter-deposited ITO top electrodes through a shadow mask with 100 μm diameter holes. The capacitance−voltage (C−V) was measured using an HP 4284A impedance analyzer over the frequency range of $1-10^3$ kHz. The dielectric leakage current (J_g) was investigated using an HP 4140B picoammeter/DC voltage source. The ITO top electrode was biased while the Si substrate was grounded during the electrical measurements.

For the TMO FETs, a heavily doped p-type silicon wafer was used as the bottom gate electrode. The IZO thin film was deposited as the channel layer on the SiO_2/Si, $LaZrO_x$/Si and $LaZrO_x/SiO_2$/Si substrates by direct current (dc) magnetron sputtering. The working

pressure and dc power during the sputtering of IZO (60 wt % In) were 100 W and 2 mTorr, respectively, under an Ar atmosphere. The ITO film as a source/drain (S/D) electrode was deposited using an identical sputtering system with an ITO target composition of 90 wt % In and 10 wt % Sn. During deposition of the ITO S/D electrode (90 wt % In), the working pressure and dc power were 5 mTorr and 50 W, respectively, under an Ar atmosphere. The width (W) and length (L) of the channel region in the fabricated IZO FETs were 100 and 150 μm, respectively. The isolated channel and S/D electrodes were patterned through a shadow mask during sputtering deposition. The IZO FETs were annealed in air for 1 h at 180 °C. The electrical characteristics of the FETs were measured using a Keithley 2636 Source Meter at room temperature.

3. RESULTS AND DISCUSSION

Thermogravimetric analysis (TGA) was performed to monitor the effects of the catalyst on the thermal decomposition behavior of the PHPS solution, as shown in Figure 1. The

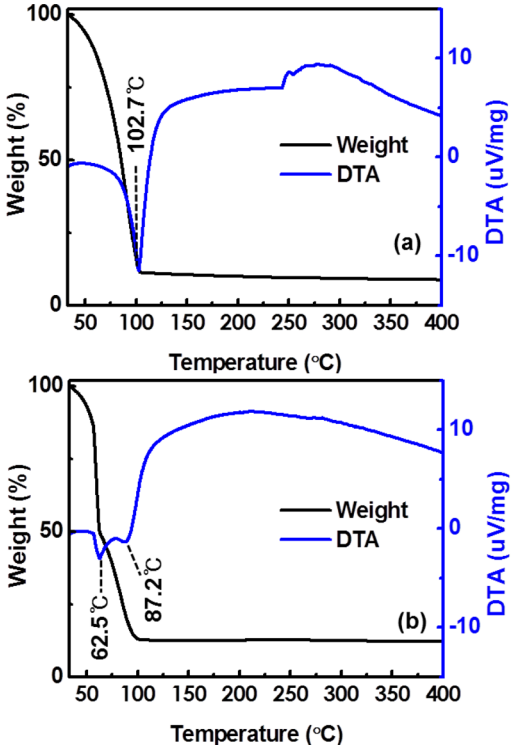

Figure 1. Thermogravimetric analysis (TGA) and differential thermal analysis (DTA) curves of the PHPS solution (a) without and (b) with the catalyst of the 2-dimetylamino-1-propanol (0.6 wt %).

weight loss observed below 100 °C for the catalyst-free PHPS solution was attributed to the evaporation of both the solvent and organic molecules including nitrogen and hydrogen incorporated into the PHPS solution (Figure 1a). The endothermic reaction near ~102.7 °C in differential thermal analysis (DTA) can be attributed to the hydrolysis of Si−N bonds and the decomposition of PHPS macro-molecules. Interestingly, the PHPS solution with the DMAPO catalyst (0.6 wt %) was decomposed at temperatures lower than that of the PHPS film without a catalyst, which was consistent with the lower endothermic reaction temperature of 62.5 °C in the DTA data (Figure 1b). Therefore, it is expected that the nitrogen atom in the PHPS substance decomposed with the DMAPO catalyst and can be replaced by an oxygen atom from the air, leading to the formation of Si−O bonds at low temperatures (<100 °C).

Figure 2 shows the FTIR spectra of the PHPS films at different curing temperatures. The spin-coated PHPS film

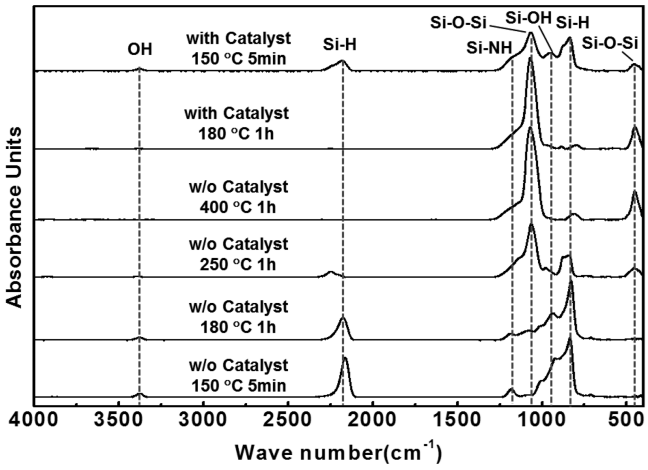

Figure 2. FTIR spectra of the PHPS films at different curing temperatures.

showed peaks at 835, 950, 2181, and 3377 cm^{-1}, which were assigned to the Si−H wagging vibration, Si−H deformation, Si−H stretching, and O−H stretching bands, respectively.[25,26] This is understandable because PHPS is an inorganic oligomer (M_n = 600−2000 g mol^{-1}, M_w = 1400−10000 g mol^{-1}) consisting of $-SiH_2NH-$ units. The bands assignable to the Si−O−Si asymmetric stretching transverse optical mode (1068 cm^{-1}) and the Si−O−Si rocking mode (451 cm^{-1}) were amplified significantly for the PHPS film cured at 400 °C, suggesting that the PHPS film is transformed completely to a condensed SiO_2 film. As the curing temperature was decreased to 180 °C, the intensity of the siloxane bond (Si−O−Si) and Si−H bond decreased drastically and increased, respectively. This suggests that it is difficult to form an amorphous Si−O network framework from traditional PHPS by low temperature curing (<250 °C). In contrast, the PHPS film from the solution with the DMAPO catalyst showed an FTIR spectrum similar to that of the SiO_2 film prepared at 400 °C. This clearly shows that the catalyst-assisted curing of the PHPS solution resulted in high-quality SiO_2 network formation at a low temperature of 180 °C.

Figure 3 presents the catalyst-assisted thermal conversion of PHPS in the presence of moisture to SiO_2.[27] DMAPO is a well-known alkaline catalyst, in which the hydroxyl group (OH) and basicity can attack the Si−N and Si−H bond, respectively. Therefore, thermal annealing of the PHPS films with a

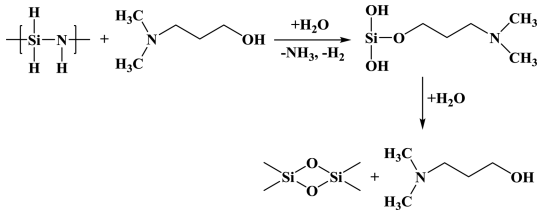

Figure 3. Schematic diagram showing the plausible reaction mechanism of the catalyst-assisted thermal conversion of PHPS in the presence of moisture to SiO_2.

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DMAPO catalyst under moisture conditions cause efficient oxidation at low temperatures, which involve the hydrolysis of Si−N and S−H bonds leading to the release of NH_3 and H_2 and the formation of silanol groups. These intermediate silanol groups are converted to a SiO_2 network by a subsequent thermally initiated condensation process during thermal annealing.

Figure 4a shows the XPS survey spectra of the SiO_2 films cured at 180 °C. The C 1s peak for C−C bonds was used to calibrate the photoelectron binding energy. The catalyst-free sample had N 1s, Si 2p, and O 1s peaks. The intensity of the N 1s and O 1s peaks for the catalyst-assisted SiO_2 film decreased and increased significantly, respectively, compared to those for the catalyst-free sample. In Figure 4, panels b and c present the O 1s XP spectra of the catalyst-free and -assisted SiO_2 films, respectively. The O 1s peaks can be deconvoluted into 531.7 and 532.6 eV. The peaks at 531.7 and 532.6 eV were assigned to the O−Si lattice peak and OH impurity, respectively.[28] The relative area of the O−Si-lattice-related peak for the catalyst-free and -assisted SiO_2 film were 54.0 and 62.8%, respectively, as summarized in Table 1. In contrast, the hydroxyl group related peak area of the catalyst-assisted SiO_2 was diminished from 46.0 (catalyst-free SiO_2) to 37.2%. In Figure 4, panels d and e show the Si 2p XPS for the catalyst-free and assisted SiO_2 films, respectively. In the case of the catalyst-free SiO_2 films, the rather broad Si 2p XPS can be deconvoluted into the SiO_2, SiO_x, Si_3N_4, and SiC-related peaks, where their corresponding peak positions were 103.8, 102.8, 102.0, and 100.6 eV, respectively.[29] The impurity-related peaks, such as Si_3N_4 and SiC bonding, disappeared in the Si 2p XP spectra of the catalysis-assisted SiO_2 film, as shown in Figure 4e. In addition, the SiO_2 and SiO_x lattice peaks of the catalysis-assisted SiO_2 film increased and deceased substantially, respectively, compared to those of the catalysis-free SiO_2 film (also see Table 1). These results suggest that the DMAPO catalyst promotes the conversion of the silazane-based precursor to the condensed SiO_2 dielectric film, which supported the interpretation based on the FTIR result.

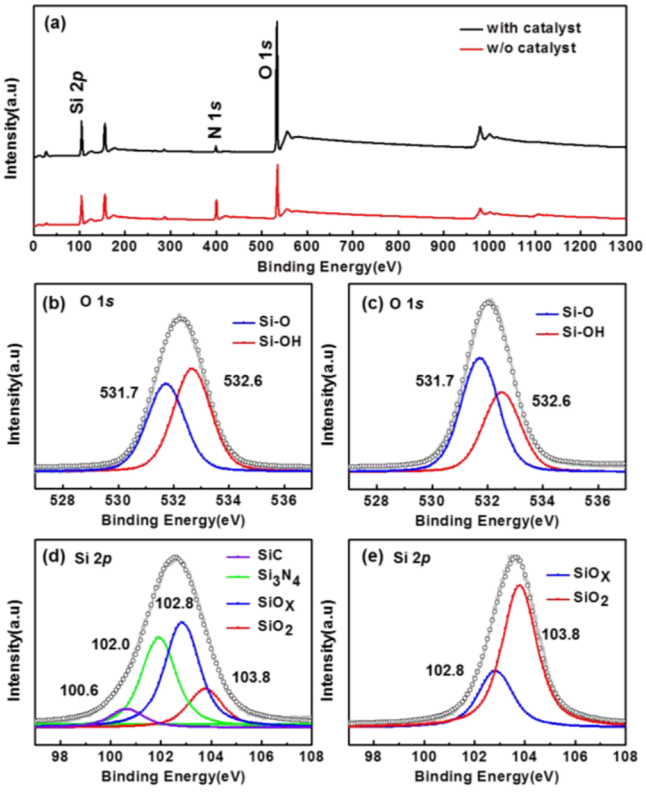

Figure 4. (a) XPS survey spectra of the SiO_2 films cured at 180 °C. XP spectra of O 1s for the (b) catalyst-free and (c) catalyst-assisted SiO_2 film. XP spectra of Si 2p for the (d) catalyst-free and (e) catalyst-assisted SiO_2 film.

In this study, high-k $LaZrO_x$ films were also prepared by spin-coating a zirconium lanthanum oxide sol−gel solution followed by annealing at temperatures ranging from 180 to 400 °C. Here, the $LaZrO_x$ dielectric was chosen because the ZrO_2 and La_2O_3 dielectrics have a wide band gap (≥5.5 eV) and high dielectric permittivity, allowing a low leakage current and low voltage driving. The cation composition ratio of La/Zr in the $LaZrO_x$ film was 0.32:0.68, which was determined by X-ray fluorescence spectroscopy. Figure 5 shows the TGA and DTA data for the dried $LaZrO_x$ precursor. The small endothermic peak near 103.8 °C was assigned to the decomposition and hydrolysis of the metal precursors.[15] The sharp exothermic reaction at 163.4 °C indicates the metal-to-oxygen (M-O) formation at a low temperature. The reason for the M-O formation such a low temperature will be discussed below. The broad exothermic peak (>200 °C) suggests gradual densifica-

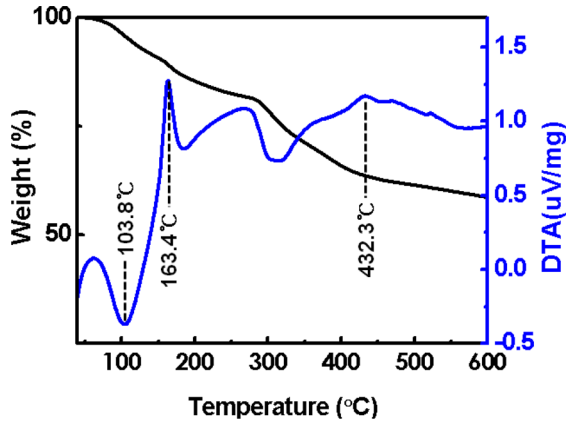

Figure 5. TGA and DTA curves for the dried $LaZrO_x$ precursor.

Table 1. Comparisons of the O 1s and Si 2p Peaks from the XPS Spectra of the Catalyst-Free and -Assisted SiO_2 Films

	Si 2p			O 1s		
	SiC	Si_xN_4	SiO_x	SiO_2	SiO_2	SiOH
catalyst-free SiO_2	100.6 eV (7.4%)	102.0 eV (41.6%)	102.8 eV (35.7%)	103.8 eV (15.3%)	531.7 eV (54.0%)	532.6 eV (46.0%)
catalyst-assisted SiO_2			102.8 eV (28.6%)	103.8 eV (71.4%)	531.7 eV (62.8%)	532.6 eV (37.2%)

tion. The exothermic reaction near 432.3 °C without weight loss corresponds to the crystallization of $LaZrO_x$.

The insulating properties of the $LaZrO_x$ films prepared at the different annealing temperatures were examined by fabricating metal−insulator−metal capacitors. The gate leakage current density (J_g) versus the applied electric field (E) of the $LaZrO_x$ dielectrics on a heavily doped Si substrate was measured using an ITO top electrode, as shown in Figure 6a. For a better

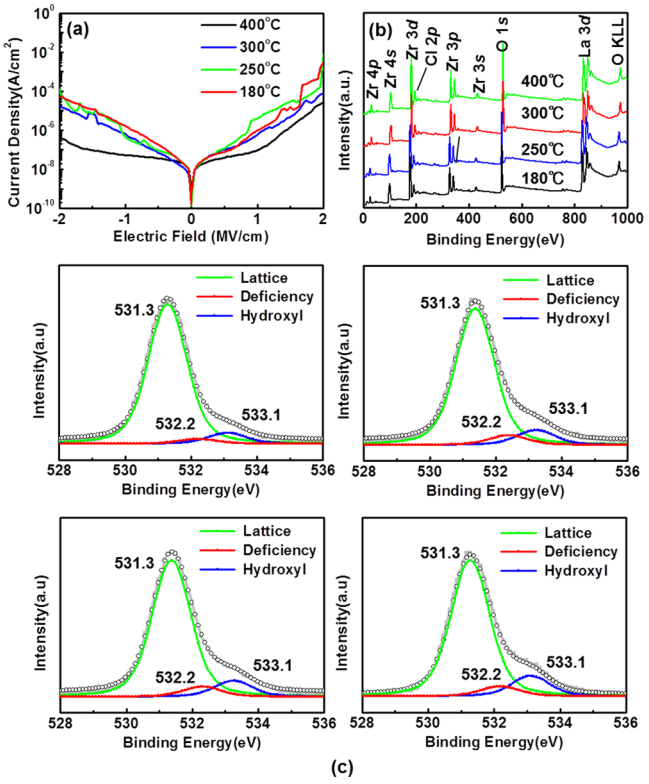

Figure 6. (a) Gate leakage current density (J_g) vs applied electric field (E) of the capacitors with the $LaZrO_x$ dielectrics at different annealing temperatures. (b) XPS survey spectra of the $LaZrO_x$ dielectrics. (c) XP spectra of O 1s for the $LaZrO_x$ dielectrics.

comparison, the J_g values of both capacitors were plotted as a function of the thickness-normalized electric field. The capacitor with the $LaZrO_x$ dielectric film prepared at 400 °C exhibited the lowest J_g of 8×10^{-8} A/cm^2 at 1 MV/cm. The J_g of the $LaZrO_x$ capacitor increased with decreasing annealing temperature. On the other hand, the J_g of $\sim 10^{-6}$ A/cm^2 at 1 MV/cm for the $LaZrO_x$ capacitor prepared at 180 °C was comparable to or even lower than those of the solution processed high-k dielectric capacitors prepared at the higher annealing temperature (≥400 °C),[13,15,17] which is acceptable for stable transistor operation. Figure 6b shows the XPS survey spectra of the solution-processable $ZrLaO_x$ films at different annealing temperatures. Zr 3d, La 3d, and O 1s peaks for all $ZrLaO_x$ films were clearly observed. Figure 6c shows the O 1s XPS of the $LaZrO_x$ films. The asymmetric O 1s peaks can also be deconvoluted into 531.3, 532.2, and 533.1 eV. The main lattice peak (531.3 eV) of O 1s is consistent with the typical O 1s peak position of stoichiometric ZrO_2 or La_2O_3. The peaks at 532.2 and 533.3 eV were assigned to the oxygen deficiency lattice peak and OH^- impurity, respectively.[30] The oxygen lattice and OH-related peaks of the $LaZrO_x$ film increased and decreased with increasing annealing temperature, suggesting that the decomposition of metal precursor, hydrolysis, and condensation reactions are thermally activated (See Table S1, Supporting Information). This is consistent with the best insulating property of the resulting capacitor. In particular, the $LaZrO_x$ film prepared at a low temperature of 180 °C still exhibited a large peak area fraction (~80%) for the oxygen lattice compared to those of the oxygen deficiency and OH impurity. The annealing temperature of the metal oxide film deposited by the sol−gel method depends strongly on the chemical bonding strength of the cation and oxygen ion, the ligand structure of metal precursor, and chemical additives.[31,32] The addition of a strong oxygen getter such as Ga reduces the annealing temperature for the solution-processable oxide materials because of its high bonding strength to the oxygen anion.[33] Similarly, the high bonding strength of Zr−O (776.1 kJ/mol) and La−O (1,170 kJ/mol) in this study would be beneficial to the formation of a M−O−M lattice at low temperatures.[34,35] Second, the annealing temperature required for the acetate-based precursor was reported to be higher (≥300 °C) because the carbon residue remained in the resulting oxide film, even after high-temperature annealing.[31,36,37] Carbon-free precursors such as zirconium chloride and lanthanum nitrate, which facilitates the efficient decomposition, hydrolysis, and condensation reaction, were used. In addition, nitric acid was added as an efficient oxidant because it easily decomposes to nitrogen dioxide and oxygen at low temperatures. This additional oxygen anion can accelerate the hydrolysis reaction of metal cations.[38]

Figure 7a,b shows the depth profiles of carbon and nitrogen in the $LaZrO_x$ film at 180 °C (also see Figure S1, Supporting

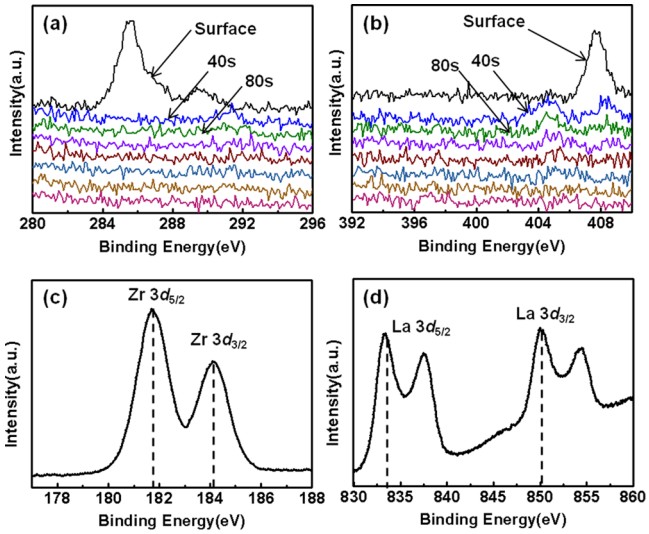

Figure 7. (a) C 1s and (b) N 1s depth profiles of the $LaZrO_x$ dielectrics film at 180 °C. XP spectra of (c) Zr 3d and (d) La 3d for the $LaZrO_x$ film at 180 °C.

Information). Indeed, the carbon and nitrogen signals were detected only on the surface of the $LaZrO_x$ film due to the inevitable surface contamination. (Figure S1, Supporting Information). These adverse impurities were not observed in the bulk of the dielectric film, suggesting that the metal precursor cleanly decomposes, even at low temperatures without organic residues detectable by XPS. Third, chlorine (Cl) incorporation in the dielectric film would be advantageous for the low leakage characteristics. All dielectric films,

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irrespective of the annealing temperatures, were in the chlorinated $LaZrO_x$ state. The atomic fraction of Cl in the $LaZrO_x$ films was 19.1−20.3%, whereas Cl ions existed uniformly in the $LaZrO_x$ films (Figure S1 and Table S2, Supporting Information). Halogen elements such as Cl or F are likely to inactivate the oxide charge trap state and reduce the fixed charges, leading to an improvement in the insulating properties of the resulting high-k dielectric oxide films such as HfO_2[39,40] and Al-doped ZrO_2.[41] The similar beneficial behavior of the halogen elements has been reported for the IZO and ZTO channel materials in which the resulting TFTs exhibited better transporting and electrical stability.[42,43] Therefore, the superior leakage characteristic of the capacitor with the $LaZrO_x$ film annealed at a low temperature of 180 °C can be attributed to the following: (1) the high bonding strength of Zr−O and La−O, (2) the use of acetate-free metal precursors, and (3) halogen incorporation to the dielectric film. Figure 7c,d shows the Zr 3d and La 3d XP spectra of the $LaZrO_x$ film at 180 °C, respectively. No metallic peak was detected in the Zr 3d and La 3d spectra of the prepared $ZrLaO_x$ films. The peaks at 181.7 and 184.1 eV, as shown in Figure 7c, were assigned to Zr $3d_{5/2}$ and $3d_{3/2}$, respectively, with a spin−orbit split of 2.4 eV, indicating the formation of ionic bonding between Zr^{4+} and O^{2-}.[44] The magnitude (~4.4 eV) of multiplet splitting of La $3d_{3/2}$ and $3d_{5/2}$ suggests that the La cation is coordinated with O^{2-} ions (Figure 7d). From XPS, the $LaZrO_x$ film was confirmed to be a completely oxidized ionic substance with a Zr−O−La bond.[45]

XTEM analysis further showed that the microstructures of the spin-coated SiO_2 and $LaZrO_x$ films were amorphous, which can be confirmed from the nanodiffraction patterns (Figure 8a, inset of Figure 8b, and Figure S2 in Supporting Information). The thickness of the SiO_2 and $LaZrO_x$ films prepared by the one-time spin-coating was 166 and 22 nm, respectively. Because the smooth dielectric/semiconductor interface is essential for the efficient transport of charge carriers in the FET device, the surface morphology and roughness were examined by AFM.

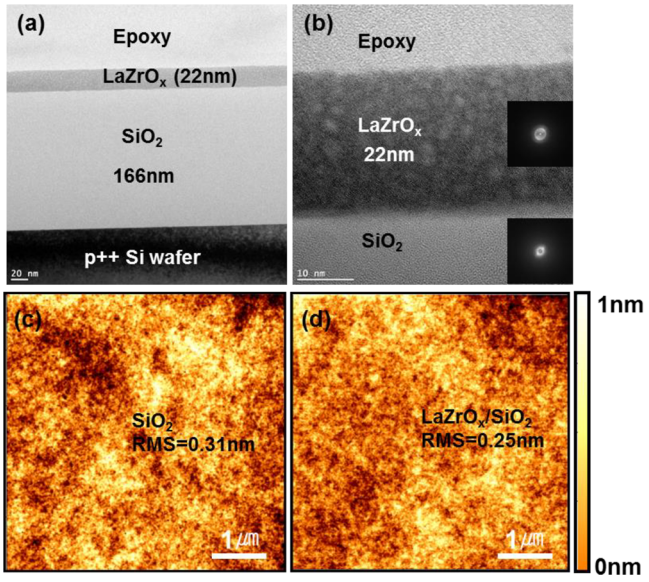

Figure 8. (a) Cross-sectional TEM image of $LaZrO_x/SiO_2$ bilayer on Si substrate. (b) Enlarged XTEM image of the $LaZrO_x/SiO_2$ dielectric film on the Si substrate. The insets show the corresponding nanodiffraction patterns of the $LaZrO_x$ and SiO_2 region with a diffuse ring. AFM images of spin-coated (c) SiO_2 and (d) $LaZrO_x/SiO_2$ film on Si substrate. The scale is 5 × 5 μm, and the height color scale is 0−2 nm.

Figure 8c,d shows AFM images of the spin-coated SiO_2 and $LaZrO_x/SiO_2$ film on the Si substrate. Smooth surfaces were obtained for both films: the root-mean-square roughness values of the spin-coated SiO_2 and $LaZrO_x/SiO_2$ films were 0.31 and 0.25 nm, respectively. Therefore, the high carrier mobility in the resulting FETs on these dielectric interfaces can be anticipated due to the elimination of surface roughness-induced carrier scattering.

The insulating properties of the SiO_2 and $LaZrO_x/SiO_2$ films were assessed by fabricating metal−insulator−metal capacitors. Figure 9a shows the J_g−E characteristics of the bare SiO_2 and $LaZrO_x/SiO_2$ dielectrics on a heavily doped Si substrate. The spin-coated SiO_2 capacitor exhibited a reasonable J_g (1.8×10^{-6} A/cm^2) at 1 MV/cm. The $LaZrO_x/SiO_2$ bilayer capacitor showed a lower J_g value of 1.6×10^{-7} A/cm^2 at the same 1 MV/cm (also see Figure S3, Supporting Information). The superior insulating property of the bilayer capacitor can be used to achieve better performance of the IZO FETs. In addition, the gate dielectric breakdown field (~5 MV/cm) of the bilayer capacitor was higher than that (~4 MV/cm) of the SiO_x capacitor (data not shown). The superior insulating property of the bilayer dielectric film compared to the single-layer dielectric can be explained using the following rationale: The second coated $LaZrO_x$ film in the bilayer dielectric film can fill the pre-existing pinholes in the underlying SiO_2 film due to local dewetting of the solution film and/or unwanted contaminations on the substrate surface. Because these pinhole defects provide a local conducting path and increase the gate leakage current, the bilayer stack of the $LaZrO_x/SiO_2$ films would result in the lower gate leakage characteristics compared to that of a single dielectric film. The similar improvement in the electrical properties using the hybrid stack was also reported in the field of organic or inorganic TFTs.[46−48]

Figure 9b shows the areal capacitance versus frequency characteristics of the bare SiO_2 and $LaZrO_x/SiO_x$ bilayer dielectrics capacitors. The capacitance of the bare SiO_2 and $LaZrO_x/SiO_2$ bilayer dielectrics at 10 kHz were ~28.2 and 25.0 nF/cm^2, respectively. It is noted that the batch-to-batch variations (1σ) of the capacitances for the SiO_2 and $LaZrO_x/SiO_2$ at 10 kHz were 27.6 ± 3.3 and 23.8 ± 2.5 nF/cm^2, respectively (Figure S4, Supporting Information). It gives rise to the corresponding variations in the field-effect mobility for the IZO FETs with the SiO_2 and $LaZrO_x/SiO_2$ by approximately 13% and 12%, respectively (Figure S4, Supporting Information). The slightly lower capacitance of the $LaZrO_x/SiO_2$ bilayer dielectrics can be understood by considering a series capacitor model ($1/C_{total} = 1/C_{SiO_2} + C_{LaZrO_x}$). The extracted relative dielectric constant of the spin-coated SiO_2 and $LaZrO_x$ film were 5.3 and 11.8, respectively.

IZO FETs with SiO_2 and $LaZrO_x/SiO_2$ bilayer insulators were fabricated. In Figure 10, panels a and c show the transfer characteristics of the IZO FETs with SiO_2 and $LaZrO_x/SiO_2$ bilayer insulators, respectively. The field-effect mobility (μ_{FE}) was determined from the incremental slope of the $I_{DS}^{1/2}$ versus V_{GS} plot in the saturation region using the following equation:

$$I_{DS} = (WC_i/2L)\mu_{FE}(V_{GS} - V_{TH})^2 V_{DS} \quad (1)$$

where L is the channel length, W is the width, and C_i is the gate capacitance per unit area. V_{TH} was defined as the gate voltage

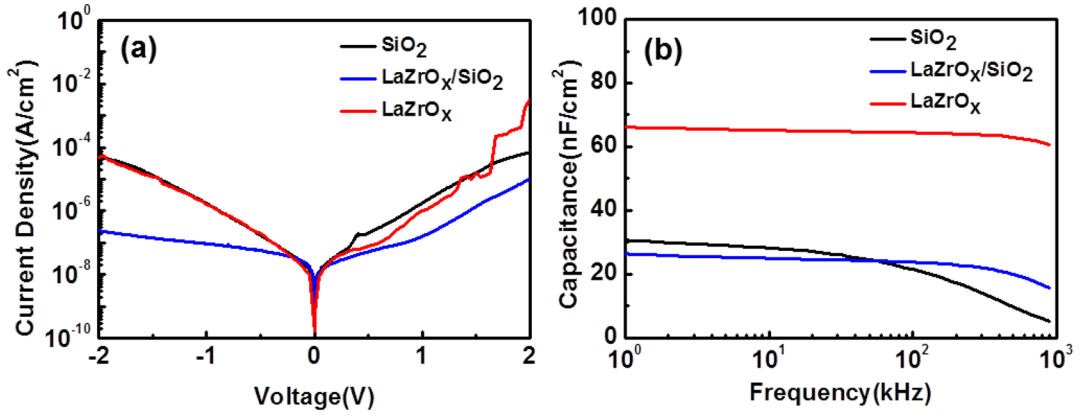

Figure 9. (a) J_g–E characteristics of bare SiO_2 and $LaZrO_x/SiO_2$ dielectrics on a heavily doped Si substrate. (b) Areal capacitance vs frequency characteristics of bare SiO_2 and $LaZrO_x/SiO_2$ bilayer dielectrics capacitors.

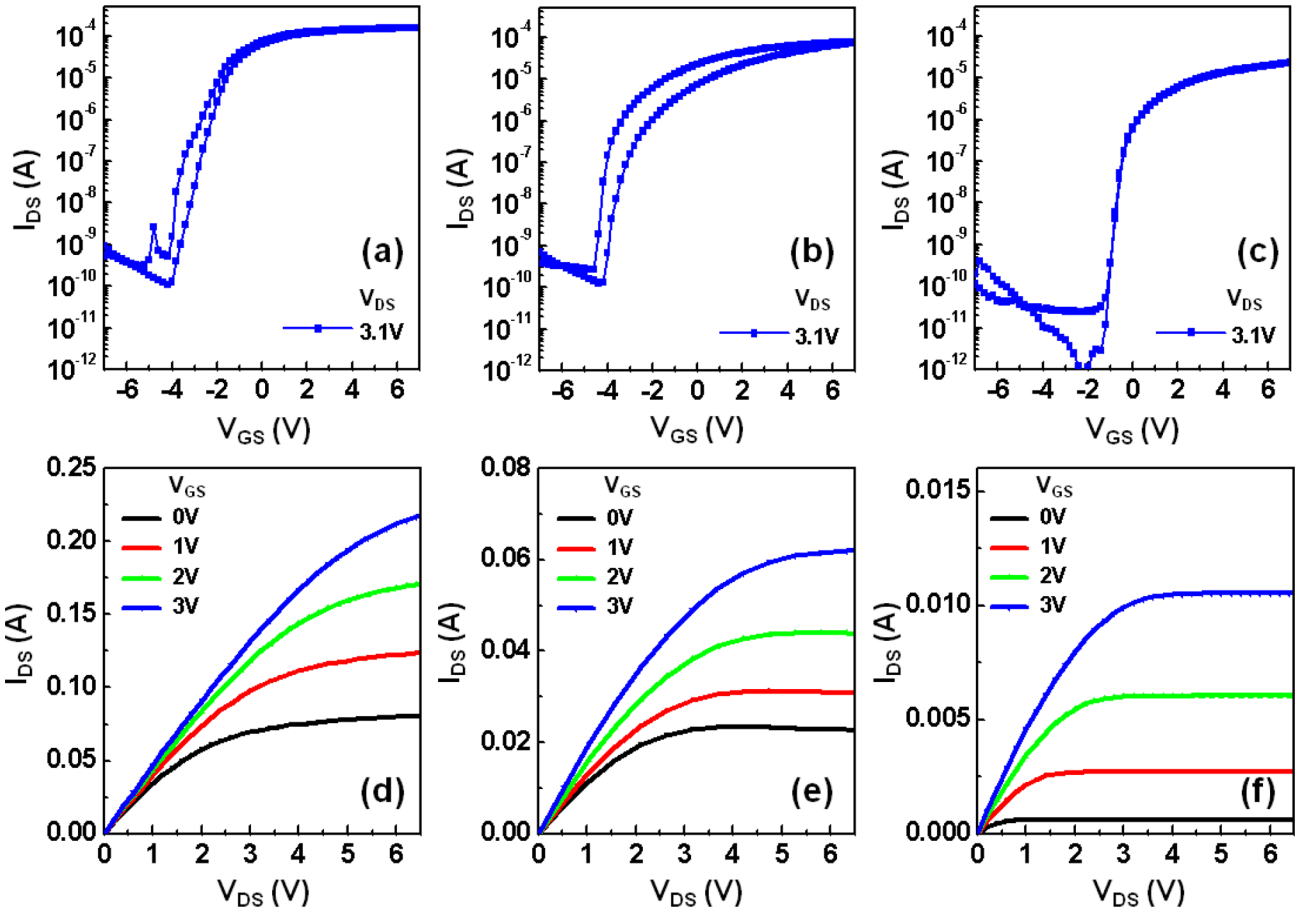

Figure 10. Representative transfer characteristics of the IZO FETs with the (a) SiO_2 (166 nm), (b) $LaZrO_x$ (160 nm), and (c) $LaZrO_x$ (22 nm)/SiO_2 (166 nm) bilayer insulators. Representative output characteristics of the IZO FETs with the (d) SiO_2, (e) $LaZrO_x$, and (f) $LaZrO_x/SiO_2$ bilayer insulators.

Table 2. Electrical Characteristics of FETs based on Different Gate Insulators[a]

FET samples	M_{Fe} ($cm^2V^{-1}S^{-1}$)	SS (V/decade)	V_{TH} (V)	I_{ON}/I_{OFF}	N_{IT} (cm^{-2})	$\Delta\nu_{Hysteresis}$ (V)
SiO_2	261.6	0.45	−3.3	2×10^6	2.1×10^{12}	0.66
$LaZrO_x$	45.8	0.27	−3.7	8×10^5	1.8×10^{12}	0.8
$LaZrO_x/SiO_2$	24.8	0.16	−0.8	4×10^7	4.1×10^{11}	~0

[a]The uniformity of the transfer characteristics for the SiO_2 and bilayer-gated IZO FETs are also shown in Figure S5 (Supporting Information).

that induces a drain current of 1 nA at V_{DS} = 3.1 V. The subthreshold gate swing [SS = $dV_{GS}/(d \log I_{DS})$ (V/decade)] was extracted from the linear part of the $\log(I_{DS})$ versus V_{GS} plot. The IZO FETs with a SiO_2 gate insulator showed

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promising performance with a high μ_{FE} of 261.6 $cm^2/(V\ s)$, a SS of 0.45 V/decade, a V_{TH} of −3.25 V, and a $I_{ON/OFF}$ ratio of 2×10^6, as summarized in Table 2. The exceptional apparent high mobility for the SiO_2 gated IZO FET should be considered carefully. The field-effect mobility extracted in this study was determined by the V_{GS}-dependent drain current variation. In the case of a relatively leaky dielectric film, the gate leakage current is reflected in the drain current, which amplifies the field-effect mobility. The possibility of n-type doping due to the reaction of a hygroscopic SiO_2 film cannot be excluded as a plausible reason for this high mobility. The water molecules that were taken up by the hygroscopic silazane-derived SiO_2 film can increase the electron carrier density of the IZO channel layer because they can play the role as an electron donor in the Zn-based oxide film.[49] Thus, the hygroscopic SiO_2-gated IZO FETs showed large batch-to-batch variations in terms of device parameters such as μ_{FE}, SS, V_{TH}, and $I_{ON/OFF}$ ratio (see Figure S5, Supporting Information). The pixel switching or driving FETs in the practical active-matrix flexible display requires high mobility and extremely low leakage drain current (<10 pA). In the case of mobile display/electronics, the leakage drain current (I_{OFF}) should be kept to a minimum because it adversely affects the power consumption. Unfortunately, the I_{OFF} of IZO FETs with a SiO_2 dielectric was rather large (~80 pA), which requires improvement. In contrast, significant improvement in terms of I_{OFF}, SS, and $I_{ON/OFF}$ ratio was observed for the IZO FETs with a $LaZrO_x/SiO_2$ bilayer dielectric: I_{OFF}, SS, and $I_{ON/OFF}$ ratio were improved to 2 pA, 0.16 V/decade, and 4×10^7, respectively, whereas a high mobility of 24.8 $cm^2/(V\ s)$ was still maintained. In addition, the batch-to-batch parameter variations for the IZO FETs with a $LaZrO_x/SiO_2$ bilayer dielectric were diminished compared to those with a single SiO_2 dielectric (See Figure S5, Supporting Information). The high mobility and good $I_{ON/OFF}$ ratio of the IZO FETs with a $LaZrO_x/SiO_2$ bilayer at 180 °C can be attributed to the low effective electron mass in an indium-based oxide, the efficient intercalation (percolation path) of the 5s orbital of In^{3+} ion, the good insulating property of the bilayer dielectric film, and the smooth IZO/$LaZrO_x$ interface. Figure 10d,f shows the representative output characteristics of the IZO FET with the SiO_2 and $LaZrO_x/SiO_2$ bilayer insulators, respectively. The clear pinch-off for both devices suggests that electron transport in the IZO active channel was controlled by the gate and drain voltages. In addition, the absence of crawling in the I_{DS} in the low V_{DS} voltage region suggested Ohmic contact between the IZO channel and ITO source/drain electrode.

The operational device stability of a given FET is often characterized by the amount of hysteresis between the forward and reverse sweep. In the case of IZO FETs with a SiO_2 dielectric, clockwise hysteresis phenomena (ΔV_{TH} = 0.66 V) were observed, as shown in Figure 10a. This hysteresis can be attributed to either carrier trapping at the interfacial trap states or carrier injection to the bulk region of the underlying dielectric film under the accumulation mode. The hydroxyl group in the oxide dielectric film is the carrier trapping center.[50−52] The presence of a hydroxyl group in the polymer-derived gate dielectric for the organic TFTs was also reported to accelerate the charge trapping phenomena for the transporting carriers, hence the hysteresis instability.[53−58] Therefore, the high concentration of the hydroxyl group in the silazane-derived SiO_2 dielectric film would be responsible for the interior hysteresis behavior. For this reason, the resistance of the SiO_2-gated IZO FETs upon humidity exposure is expected to be low due to the hygroscopic behavior of the silazane-derived SiO_2 material. In contrast, this hysteresis was reduced substantially in the IZO FETs with a $LaZrO_x/SiO_2$ bilayer dielectric, suggesting a decrease in the interfacial trap states by the introduction of a high-k $LaZrO_x$ dielectric (see Figure 10c). The denser $LaZrO_x$ film in the bilayer dielectric film may alleviate the adverse direct carrier trapping from the channel region to the bulk region of SiO_2 film. On the other hand, the pinhole-less or free structure in the hybrid stack can contribute partially to the reduction in the hysteresis. This synergic effect of the bilayer dielectric structure compared to the single layer dielectric structure in terms of the reduced gate leakage current and hysteresis has been also reported for organic thin-film transistors (TFTs).[59] The interfacial traps density (N_{it}) was calculated using the following equation from the subthreshold swing:[60]

$$N_{it} = [SS \log(e)/(k_B T/q) - 1]\frac{C_i}{q} \quad (2)$$

where q is the electron charge, k_B is the Boltzmann constant, and T is the absolute temperature. The calculated N_{it} value for the IZO FETs with a SiO_2 and $LaZrO_x/SiO_2$ dielectric were 2.4×10^{12} and 4.1×10^{11} $/cm^2$, respectively. Therefore, the superior operational stability of the IZO FETs with a bilayer dielectric is well corroborated with the lower N_{it} value. This suggests that the role of the $LaZrO_x$ dielectric is to provide better interface matching between the IZO channel layer and gate dielectric layer, thereby allowing a decreased N_{it} value and good operational stability of the resulting FETs.

Generally, high-k dielectrics such as HfO_2, ZrO_2, La_2O_3 are preferred as a gate insulator owing to their excellent charge coupling capability, which results in a decreasing SS factor and low operating voltage. On the other hand, the high-k dielectric suffered from a high leakage current and low breakdown voltage because they have a lower band gap and smaller band offsets to the metal oxide semiconductor compared to SiO_2 or Al_2O_3 dielectrics.[61,62] These adverse electrical properties can be aggravated further by the polycrystalline nature, where the grain boundary defects act as a leakage current path. In this regard, this study also examined the device performance of the IZO FETs with a $LaZrO_x$-only gate insulator, where the $LaZrO_x$ films of greater thickness (~160 nm) can be obtained by 6 times spin-on deposition and annealing at 180 °C. Although a high mobility of 45.8 $cm^2/(V\ s)$ was obtained, they suffered from a larger I_{OFF} value (100 pA) and inferior hysteresis (ΔV_{TH} = 0.8 V; Figure 10b). Therefore, the promising performance of the IZO FETs with a $LaZrO_x/SiO_2$ bilayer dielectric is the synergistic effects of the PHPS-derived SiO_2 film with good bulk property and a sol−gel-derived $LaZrO_x$ film with better interfacial matching. Many studies have emphasized the high mobility (>50 $cm^2/(V\ s)$) of the TMO TFTs.[13,63−66] On the other hand, the I_{OFF} values reported in those studies were rather high (>100 pA),[62−65] which is unacceptable for practical applications as a pixel driver. Therefore, the compromise between the field-effect mobility and I_{OFF} values achieved for the IZO FETs through the introduction of a $LaZrO_x/SiO_2$ bilayer gate dielectric will have technical implications for the realization of flexible, low-cost electronics.

4. CONCLUSION

This study showed that a PHPS-derived SiO_2 film capped with a $LaZrO_x$ dielectric film affords a smooth, pinhole-free dielectric material with high-capacitance and good insulating properties. This bilayer stack can be readily deposited from solution at a low temperature of 180 °C, which can be compatible with the plastic substrate. The resulting IZO FETs with a stack of $LaZrO_x/SiO_2$ dielectric exhibited a high mobility of 24.8 $cm^2/(V\,s)$, a low voltage driving of <5 V, a low SS factor of 0.16 *V*/decade, a high $I_{ON/OFF}$ ratio of 4×10^7, and good hysteresis-free stability. Therefore, the solution-based $LaZrO_x/SiO_2$ dielectric stack is an attractive candidate as a solution-processable gate dielectric for high-performance, low-cost, and flexible TMO FETs.

■ ASSOCIATED CONTENT

Supporting Information

Deconvolution data of XPS O1s peaks, concentration depth profiles and X-ray diffraction patterns for various $LaZrO_x$ films; statistical data on the *J*−*E* and *C*−*f* of SiO_2 and $LaZrO_x/SiO_2$ capacitors and the corresponding transfer characteristics of IZO FETs. This material is available free of charge via the Internet at http://pubs.acs.org.

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Notes

The authors declare no competing financial interest.

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